

Notice of References Cited	Application/Control No. 09/833,653	Applicant(s)/Patent Under Reexamination KAMITANI ET AL.	
	Examiner Shane F Gerstl	Art Unit 2183	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,530,011	03-2003	Choquette, Jack H.	712/3
	B	US-6,038,656	03-2000	Martin et al.	712/211
	C	US-			
	D	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	High Performance Single Chip Dataflow Processor; Kuru, G; ASIC Conference and Exhibit, 1995; 18-22 Spet 1995; pages 346-349
	V	An Advanced Dataflow Processor Architecture Based on a Multiple Input Node Concept; Kuru, G and Deshmukh, R G; Southeastcon '93; 4-7 April 1993; 8 pages
	W	COMputer Architecture, A Quantitative Approach; David A Patterson and John L Hennessy; 1990; Morgan Kaufmann Publishers; Pages 429-431
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.